Application No.: 10/035,886 Docket No.: 29926/38065

REMARKS

Claims 1-2 and 4-9 are pending, with claims 8 and 9 added by amendment above. No new matter has been added. Claims 1-2 and 4-7 stand rejected based on a single patent, Sakurai. The applicants have carefully considered the rejections and respectfully traverse, for at least the reasons outlined in the remarks below. Reconsideration and allowance in view of the following comments are respectfully requested.

Claim 1, as amended, recites an apparatus for controlling a bank refresh including a plurality of banks. The apparatus includes "a reset control unit for receiving output signals from the plurality of input buffer means to thereby generate a reset signal" and a counter for producing count signals wherein the counter is reset by the reset signal. The "reset control unit includes a NOR gate for combining the output signals from the plurality of input buffer means." Sakurai does not teach the recited subject matter.

The office action although acknowledging that Sakurai does not teach multiple banks or memory cells with a bank configuration, nonetheless rejects claim 1 as obvious. The rejection is factually unsupported, legally flawed, and thus improper.

Interestingly, the office action, while conceding that Sakurai does not specify a memory system with "a plurality of banks," points to Sakurai's discussion of Figure 15 as establishing that such a "plurality of banks" would be obvious. Yet, the description of Figure 15 clearly shows that the memory cell does not, and apparently would not, have a bank configuration:

> Since the memory array does not have the bank configuration, the semiconductor memory device controls activation/inactivation of the array instead of that of a bank by bank. Col. 19, ll. 54-57

In other words, not only does Sakurai's Figure 15 not teach a memory cell with a bank configuration, it appears to teach away from a bank configuration by the repeated statements describing the embodiment of Figure 15. Either of these points alone sufficiently demonstrates the improper nature of the office action's obviousness rejection. And either of these points alone establishes that the rejection of claim 1 should be withdrawn.

Yet, Sakurai is deficient in other ways as well. Sakurai, for example, does not teach "a reset control unit for receiving output signals from the plurality of input buffer means to thereby generate a reset signal," as recited in claim 1. The refresh control circuit 18 of Sakurai receives a single input (Φr) that has been determined by the command decoder 5 based on the control signals from control signal buffer 7. In detail, the command decoder 5 outputs the refresh mode instruction signal Φr to the refresh control circuit 18. Then, the refresh counter, generating a refresh command signal RADi, is controlled by the refresh control circuit 18. That is, Sakurai's refresh control circuit does not receive output signals from a "plurality of input buffer means," but rather requires a command decoder circuit to create the refresh instruction signal (Φr) to be used by the refresh control circuit. Furthermore, there is no suggestion of a reset control unit that includes a NOR gate for combining the output signals from the plurality of input buffer means," as recited in claim 1.

In contrast, page 5, lines 13 to 26 of the present application describes an example reset control unit including a multiple-input NOR gate and an inverter, where the reset signal is generated by logic NOR operation based on output signals from a plurality of input buffer means. Also, the counter for determining a timing of the refresh operation starts counting in response to the reset signal outputted from the reset control unit (See, e.g., page 6, line 18 to page 7, line 12). That is, the example reset control unit is more effective and simpler than the command decoder 5 and the refresh control circuit 18 of Sakurai.

In any event, Sakurai does not teach "a reset control unit for receiving output signals from the plurality of input buffer means to thereby generate a reset signal," as recited in claim 1. And there is no teaching, suggestion, or motivation from the prior art to modify Sakurai to have such a reset control unit.

For at least the reasons outlined above, the obviousness rejection of claim 1 is traversed. Claim 1 and claims 2, 4-6[1], 8 and 9 are in condition for immediate allowance.

Claim 5 recites, in part, buffering N bank address signals inputted from the external circuit with the refresh command signals and generating a reset signal

[1] The applicant notes that the office action mistakenly rejects claim 6 as depending from method claim 5, when in fact claim 6 depends from apparatus claim 1.

based on the logic NOR operation of the N buffered bank address signals. Sakurai does not disclose or suggest the recited subject matter.

The office action takes the position that:

> Although the number of banks ("memory arrays") is not specified, the system can be configured to comprise a plurality of banks as well as a plurality of buffer means (See Figure 15 and Column 19, lines 15-37).

First, as a procedural matter, whether something is feasible or not is not the test for *prima facie* obviousness. To establish *prima facie* obviousness, there must be some teaching, suggest, or motivation from the prior art to make the proposed combination or modification. One cannot rely upon the mere fact that references can be combined or modified, unless the prior art also suggests the desired combination. MPEP §2143.01, citing In re Mills, 916 F.2d 860 (Fed. Cir. 1992). Nor may one maintain a rejection based on the notion that the claimed subject matter was within the capabilities of one of ordinary skill in the art. Ex parte Levengood, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993) (stating that a rejection that the claimed inventions would have been well within the ordinary skill of the art at the time the invention was made is not sufficient to establish a *prima facie* case of obviousness). The office action fails to provide any *prima facie* showing and, thus, is improper on its face.

Second, as a substantive matter, the applicants have recited above that Sakurai does note teach the recited subject matter. Figure 15 is specifically described as not having a bank configuration. The description at column 19, lines 15-37 does describe array banks (0-3) for the embodiment of Figure 14. Yet, while Sakurai shows array banks (0-3), it shows them in a device without any need for a plurality of buffer means. If Sakurai provides any teaching or suggestion, it is away from using both an array bank and a plurality of buffer means. Furthermore, no where does Sakurai teach or suggest generating a reset signal based on the logic NOR operation of N buffered bank address signals.

In short, the rejection of claim 5 is traversed. Claim 5 and claim 7 depending therefrom are in condition for immediate allowance.

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In view of the above remarks, each of the presently pending claims 1-2 and 4-9 are believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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